Patent Abstracts of Japan

PUBLICATION NUMBER : 03205868
PUBLICATION DATE : 09-09-91

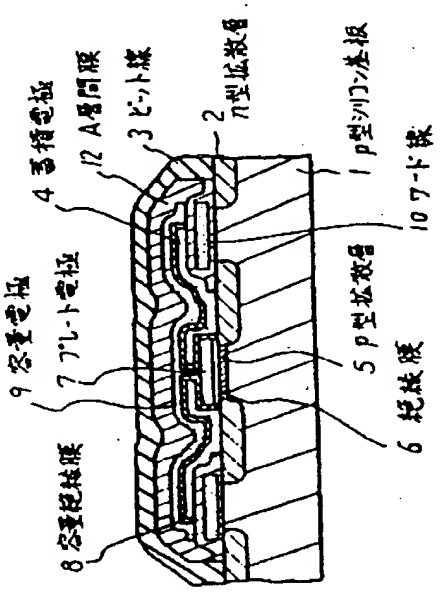
APPLICATION DATE : 08-01-90
APPLICATION NUMBER : 02001867

APPLICANT : NEC CORP;

INVENTOR : NAKAMURA KUNIO;

INT.CL. : H01L 27/108 H01L 21/76

TITLE : MIS TYPE SEMICONDUCTOR MEMORY



ABSTRACT : PURPOSE: To increase a memory cell capacity and to improve the stable operation and yield of an element by electrically isolating between the cells by fixing the potential of a plate electrode provided on a substrate between the cells to a predetermined potential.

CONSTITUTION: In a MIS type semiconductor memory for forming one memory cell of one insulated gate field effect transistor, and a capacity formed by laminating at least two conductive layers on a substrate, the same conductivity type impurity diffused layer 5 as the substrate 1 is formed on the substrate of an isolating region between elements between the cells, a plate electrode 7 for isolating between elements is formed on the substrate 1 on the layer 5 through an insulating film 6, the potential of the electrode 7 is fixed to a predetermined potential, and a capacity is formed between the electrodes 4 and 7 through an insulating film 8. For example, the potential of the electrode 7 is grounded or fixed to a suitable potential.